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10/820,463	04/08/2004	Graeme Storm	02EDI46752636	7260

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EXAMINER	
GILES, NICHOLAS G	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
08/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/820,463	STORM ET AL.	
	Examiner	Art Unit	
	NICHOLAS G. GILES	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Please note that the examiner has changed.

Response to Arguments

2. Applicant's arguments filed 05/22/2008 have been fully considered but they are not persuasive.

Applicant argues that Kozlowski's differential circuit is not a calibration circuit. The examiner points out that in 4:42-45 that the amplifier speeds up the load FET's self-adjustment process in turn acting as a calibration circuit.

Applicants arguments regarding the Kakaumoto reference and the calibration circuit are moot based on the response above.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 11, 20, 21, and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,929,434 to *Kozlowski et al.* in view of Official Notice.

As for **claim 11**, *Kozlowski et al.* disclose an image sensor comprising:

an array of pixels **FIG 7**, each pixel **10 and 17** comprising

a photodiode **10**,

a semiconductor device having a capacitance **FIG 1:12** and being connected to said photodiode (Column 3, lines 26-29) and operating based upon a sub-threshold

(Column 4, lines 10-12) for providing a signal that is proportional to a logarithm of light intensity on said photodiode (Column 5, lines 45-48), and

a calibration circuit **FIG 6** having a capacitance which is stated to be useable in the circuit of **FIG 1** in place of **FIG 1:16** (Column 6, lines 52-53) and for applying a voltage across the capacitance associated with said semiconductor device and said calibration circuit for producing a current within said pixel (Column 6, lines 52-63).

The *Kozlowski* reference however fails to teach that the reference voltage in use has a constant rate of change and produces a constant current.

Official Notice is taken that both the concept and the advantages of providing a voltage with a constant rate of change, such as a ramp voltage, as the reference voltage **Vref** for **FIG 6** is well known and expected in the art. Also since the current is dependent on the capacitance and the rate of change of the voltage we would have a constant current. It would have been obvious to one or ordinary skill in the art prior to applicant's invention to use a voltage with a constant rate of change, such as a ramp voltage, for the motivation of steady change and stability in the feedback loop.

As for **claim 20**, *Kozlowski et al.* disclose an image sensor comprising:

an array of pixels **FIG 7**, each pixel **10 and 17** comprising

a photodiode **10**,

a semiconductor device having a capacitance **FIG 1:12** and being connected to said photodiode (Column 3, lines 26-29); and

a calibration circuit **FIG 6** having a capacitance which is stated to be useable in the circuit of **FIG 1** in place of **FIG 1:16** (Column 6, lines 52-53) and for applying a

voltage across the capacitance associated with said semiconductor device and said calibration circuit for producing a current within said pixel (Column 6, lines 52-63).

The *Kozlowski* reference however fails to teach that the voltage produces a constant current.

Official Notice is taken that both the concept and the advantages of providing a voltage with a constant rate of change, such as a ramp voltage, as the reference voltage **Vref** for **FIG 6** is well known and expected in the art which would in turn produce a constant current, since the current is dependent on the capacitance and the rate of change of the voltage we would have a constant current. It would have been obvious to one or ordinary skill in the art prior to applicant's invention to use a voltage with a constant rate of change, such as a ramp voltage, for the motivation of steady change and stability in the feedback loop.

As for **claim 21**, *Kozlowski et al.* disclose an image sensor according to claim 20, wherein the image sensor is operating in a logarithmic mode (Column 4, lines 10-12 and Column 5, lines 45-48).

As for **claim 30**, *Kozlowski et al.* disclose a method for calibrating an image sensor operating in a logarithmic mode (Column 5, lines 45-48 and Column 6, line 52 - Column 7, line 8), the image sensor comprising an array of pixels **FIG 7**, each pixel comprising a photodiode **10**, a semiconductor device having a capacitance **FIG 1:12** and connected to the photodiode (Column 3, lines 26-29), and a calibration circuit **FIG 6** having a capacitance which is stated to be useable in the circuit of **FIG 1** in place of **FIG**

1:16 (Column 6, lines 52-53) and being connected to the semiconductor device as can be seen in **FIG 1**, the method comprising:

applying a voltage across the capacitance associated with the semiconductor device and the calibration circuit for producing a current within the pixel during calibration (Column 6, lines 52-63).

The *Kozlowski* reference however fails to teach that the reference voltage in use has a constant rate of change and produces a constant current.

Official Notice is taken that both the concept and the advantages of providing a voltage with a constant rate of change, such as a ramp voltage, as the reference voltage **Vref** for **FIG 6** is well known and expected in the art. Also since the current is dependent on the capacitance and the rate of change of the voltage we would have a constant current. It would have been obvious to one or ordinary skill in the art prior to applicant's invention to use a voltage with a constant rate of change, such as a ramp voltage, for the motivation of steady change and stability in the feedback loop.

5. **Claims 12-19, 22-29, and 31-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,929,434 to *Kozlowski et al.* in view of US Publication No. 2003/0214591 A1 to *Kakumoto, Tomokazu.*

As for **claim 12**, an image sensor according to claim 11 was disclosed by the *Kozlowski* reference, however it failed to teach one wherein each pixel further comprises a switching device between said photodiode and said semiconductor device,

said switching device being operable during calibration for isolating said photodiode from said semiconductor device.

Kakumoto, Tomokazu, however, teaches this aspect, as can be seen in **FIG 2:T1** and discussed in **Paragraphs 41 and 45**.

The *Kozlowski* reference and the *Kakumoto* reference are analogous arts because both are in the same field of endeavor of producing a voltage that is logarithmically proportional to a photocurrent. It would have been obvious to one of ordinary skill in the art prior to applicant's invention to apply the switching device taught in the *Kakumoto* reference onto the invention of the *Kozlowski* reference for the motivation of isolating any photocurrents from entering during the stabilizing of the calibration.

As for **claim 13**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 12, wherein said calibration circuit comprises an amplifier **FIG 6** having an inverting input **74** for receiving the signal from said semiconductor device **V.**, a non-inverting input **72** for receiving a reference voltage $\mathbf{V_{ref}}$, and an output $\mathbf{V_o}$ for providing a pixel output signal.

As for **claim 14**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 13, wherein the reference voltage comprises a ramp voltage for providing the voltage having the constant rate of change was discussed in the rejection to claim 11.

As for **claim 15**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 14, but fails to teach one wherein the

ramp voltage is also applied at a beginning of an image-capturing operation of said pixel.

It would however have been obvious to one of ordinary skill in the art to apply the reference voltage, which has been established that it could be a ramp voltage, at the beginning of an image-capturing operation for the motivation of keeping the amplifier balanced from the start without having to rely completely on the Wilson load of **FIG 6** in the *Kozlowski* reference, as *Kozlowski* has discussed that the more negative the input voltage is to the quiescent case the more unbalance the amplifier becomes (Column 6, line 64 - Column 7, line 8). So by applying the ramp voltage since the beginning, the quiescent case can be altered.

As for **claim 16**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 13, further comprising a feedback loop between the output of said amplifier and said semiconductor device as can be seen in **FIG 1:16** of the *Kozlowski* reference, the feedback loop for controlling said semiconductor device as can be seen in **FIG 1** that the output is connected to the gate of the semiconductor device **12**.

As for **claim 17**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 13, wherein each pixel has an image area associated therewith as can be seen in **FIG 7**. However, the *Kozlowski* reference in view of the *Kakumoto* reference fails to teach an image sensor where the amplifier for each respective pixel is completely within the corresponding image area. However, it would have been an obvious matter of design preference to put the amplifier completely

within the corresponding image area, completely outside of it, or partly within it, in order to accommodate to different structural desires, and since applicant has not disclosed that putting the amplifier completely within the corresponding image area solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the amplifier placed anywhere else. Absent any convincing showing of the criticality of the design, this particular design is nothing more than the inventor's choice without thereby departing from the scope of the invention. *In re Dailey, 149 USPQ 47 (CCPA 1976)*.

As for **claim 18**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 13, wherein each pixel has an image area associated therewith as can be seen in **FIG 7**. However, the *Kozlowski* reference in view of the *Kakumoto* reference fails to teach an image sensor where the amplifier for each respective pixel is partly within the corresponding image area. However, it would have been an obvious matter of design preference to put the amplifier completely within the corresponding image area, completely outside of it, or partly within it, in order to accommodate to different structural desires, and since applicant has not disclosed that putting the amplifier partly within the corresponding image area solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the amplifier placed anywhere else. Absent any convincing showing of the criticality of the design, this particular design is nothing more than the inventor's choice without thereby departing from the scope of the invention. *In re Dailey, 149 USPQ 47 (CCPA 1976)*.

As for **claim 19**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses an image sensor according to claim 13, wherein said semiconductor device **FIG 1:12** of the *Kozlowski* reference comprises a transistor **12** comprising a conducting terminal **24**, and wherein the capacitance is provided by a capacitance of the conducting terminal and a capacitance of the inverting input of said amplifier (between **24 and 25**) which would be evident when the switching device as discussed in claim 12 is switched to isolate **24 and 25** from the photocurrent.

As for **claim 22**, an image sensor according to claim 20, wherein each pixel further comprises a switching device between said photodiode and said semiconductor device, said switching device being operable during calibration for isolating said photodiode from said semiconductor device. See similar rejection to claim 12.

As for **claim 23**, an image sensor according to claim 20, wherein said calibration circuit comprises an amplifier having an inverting input for receiving the signal from said semiconductor device, a non-inverting input for receiving a reference voltage, and an output for providing a pixel output signal. See similar rejection to claim 13.

As for **claim 24**, an image sensor according to claim 23, wherein the reference voltage comprises a ramp voltage for providing the voltage having the constant rate of change. See similar rejection to claim 14.

As for **claim 25**, an image sensor according to claim 24, wherein the ramp voltage is also applied at a beginning of an image-capturing operation of said pixel. See similar rejection to claim 15.

As for **claim 26**, an image sensor according to claim 23, further comprising a feedback loop between the output of said amplifier and said semiconductor device, the feedback loop for controlling said semiconductor device. See similar rejection to claim 16.

As for **claim 27**, an image sensor according to claim 23, wherein each pixel has an image area associated therewith, and said amplifier for each respective pixel is completely within the corresponding image area. See similar rejection to claim 17.

As for **claim 28**, an image sensor according to claim 23, wherein each pixel has an image area associated therewith, and wherein said amplifier for each respective pixel is partly within the corresponding image area. See similar rejection to claim 18.

As for **claim 29**, an image sensor according to claim 23, wherein said semiconductor device comprises a transistor comprising a conducting terminal, and wherein the capacitance is provided by a capacitance of the conducting terminal and a capacitance of the inverting input of said amplifier. See similar rejection to claim 19.

As for **claim 31**, a method according to claim 30 was disclosed by the *Kozlowski* reference, however it failed to teach one wherein each pixel further comprises a switching device between the photodiode and the semiconductor device where the method further comprises operating the switching device during calibration for isolating the photodiode from the semiconductor device.

Kakumoto, Tomokazu, however, teaches this aspect, as can be seen in **FIG 2:T1** and discussed in **Paragraphs 41 and 45**.

The *Kozlowski* reference and the *Kakumoto* reference are analogous arts because both are in the same field of endeavor of producing a voltage that is logarithmically proportional to a photocurrent. It would have been obvious to one of ordinary skill in the art prior to applicant's invention to apply the switching device taught in the *Kakumoto* reference onto the invention of the *Kozlowski* reference for the motivation of isolating any photocurrents from entering during the stabilizing of the calibration.

As for **claim 32**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 31, wherein the semiconductor device operates based upon a sub-threshold (Column 4, lines 10-12) for providing a signal that is proportional to a logarithm of light intensity on the photodiode (Column 5, lines 45-48), and the calibration circuit comprises an amplifier **FIG 6** having an inverting input **74** for receiving the signal from said semiconductor device **V.**, a non-inverting input **72** for receiving a reference voltage $\mathbf{V_{ref}}$, and an output $\mathbf{V_o}$ for providing a pixel output signal.

As for **claim 33**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 32, wherein the reference voltage comprises a ramp voltage for providing the voltage having the constant rate of change was discussed in the rejection to claim 30.

As for **claim 34**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 33, but fails to teach one wherein the ramp voltage is applied as the reference voltage at a beginning of an image-capturing operation of the pixel.

It would however have been obvious to one of ordinary skill in the art to apply the reference voltage, which has been established that it could be a ramp voltage, at the beginning of an image-capturing operation for the motivation of keeping the amplifier balanced from the start without having to rely completely on the Wilson load of **FIG 6** in the *Kozlowski* reference, as *Kozlowski* has discussed that the more negative the input voltage is to the quiescent case the more unbalance the amplifier becomes (Column 6, line 64 - Column 7, line 8). So by applying the ramp voltage since the beginning, the quiescent case can be altered.

As for **claim 35**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 32, wherein each pixel further comprises a feedback loop between the output of the amplifier and the semiconductor device as can be seen in **FIG 1:16** of the *Kozlowski* reference, the feedback loop for controlling the semiconductor device as can be seen in **FIG 1** that the output is connected to the gate of the semiconductor device **12**..

As for **claim 36**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 32, wherein each pixel has an image area associated therewith as can be seen in **FIG 7**. However, the *Kozlowski* reference in view of the *Kakumoto* reference fails to teach an image sensor where the amplifier for each respective pixel is completely within the corresponding image area. However, it would have been an obvious matter of design preference to put the amplifier completely within the corresponding image area, completely outside of it, or partly within it, in order to accommodate to different structural desires, and since applicant has not disclosed

that putting the amplifier completely within the corresponding image area solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the amplifier placed anywhere else. Absent any convincing showing of the criticality of the design, this particular design is nothing more than the inventor's choice without thereby departing from the scope of the invention. *In re Dailey, 149 USPQ 47 (CCPA 1976)*.

As for **claim 37**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 32, wherein each pixel has an image area associated therewith as can be seen in **FIG 7**. However, the *Kozlowski* reference in view of the *Kakumoto* reference fails to teach an image sensor where the amplifier for each respective pixel is partly within the corresponding image area. However, it would have been an obvious matter of design preference to put the amplifier completely within the corresponding image area, completely outside of it, or partly within it, in order to accommodate to different structural desires, and since applicant has not disclosed that putting the amplifier partly within the corresponding image area solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the amplifier placed anywhere else. Absent any convincing showing of the criticality of the design, this particular design is nothing more than the inventor's choice without thereby departing from the scope of the invention. *In re Dailey, 149 USPQ 47 (CCPA 1976)*.

As for **claim 38**, the *Kozlowski* reference in view of the *Kakumoto* reference discloses a method according to claim 32, wherein the semiconductor device **FIG 1:12**

of the *Kozlowski* reference comprises a transistor **12** comprising a conducting terminal **24**, and wherein the capacitance is provided by a capacitance of the conducting terminal and a capacitance of the inverting input of the amplifier (between **24 and 25**) which would be evident when the switching device as discussed in claim 31 is switched to isolate **24 and 25** from the photocurrent.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NICHOLAS G. GILES whose telephone number is (571)272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NG/
08/07/2008

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